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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/754,483	01/09/2004	Kevin Conley	SDK1P017/503	6185

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EXAMINER	
CAMPOS, YAIMA	

ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTOmail@beyerlaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/754,483	CONLEY ET AL.	
	Examiner	Art Unit	
	YAIMA CAMPOS	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *72-80* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *72-80* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. As per the instant Application having Application number 10/754,483, the examiner acknowledges the applicant's submission of the amendment dated 6/28/2010. At this point, claims 72-80 have been added, and claims 1-71 have been canceled. Claims 72-80 are pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/28/2010 has been entered.

CLAIM OBJECTIONS

3. Claim 79 is objected to because the limitation "addressing,," in line 2 appears to be a typographical error and should be corrected to read "addressing,". Appropriate correction is required.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 72-80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinomura (US 5,935,228) in view of Colligan et al. (US 6,519,762) and Suda (US 2004/0123059).

6. As per claim 72. (New) A method for operating a memory card that includes a host controller configured to communicate with a host device and that provides non-volatile data storage having an address space defined by a contiguous range of addresses:

(a) retrieving volume information from an initial volume stored in a range of addresses that is a part of the contiguous range of addresses that defines the address space; [**Shinomura discloses "the client device drivers 62 read card attribute information (tuple) from the memory in the PC card... In accordance with the contents of the tuple, each client device driver 62 ascertains whether it should drive the PC card" (col. 16, lines 5-9); when the tuple indicates a client device driver 62 may enable the PC card, the card in enabled by the client device driver 62 using 16-bit card service 61, in the DOS/Windows 3.x compatible mode (col. 16, lines 11-26) and when the tuple indicates a client device driver 53 may enable the PC card, the PC card is enabled by the 32-bit card service 51, in the Windows 95 native mode (col. 16, lines 28-64) (See fig. 2 and related text);** ***thus accessing the tuple or a portion of the non-volatile memory stating whether 16-bit file system or 32-bit file system is utilized*** **]**

(b) determining, based on the volume information, whether the initial volume uses a 16- bit addressing or uses less than the 16-bit addressing; [**Shinomura discloses 16-bit addressing (col. 7, lines 24-65) wherein when the tuple indicates a client device driver 62 may enable the PC card, the card in enabled by the client device driver 62 using 16-bit card service 61, in the DOS/Windows 3.x compatible mode (col. 16, lines 11-26)]**

(c) when said determining (b) determines the initial volume uses greater than the 16-bit addressing, communicating to the host via the host controller to use the memory card… using 32-bit addressing; and **[Shinomura discloses 32-bit addressing mode (col. 7, lines 24-65) wherein when the tuple indicates a client device driver 53 may enable the PC card, the PC card is enabled by the 32-bit card service 51, in the Windows 95 native mode (col. 16, lines 28-64) (See fig. 2 and related text)]; however, Shinomura does not expressly disclose accessing the memory card as a single volume using 32-bit addressing**

Shinomura does not expressly disclose (d) when said determining (b) determines that the initial volume uses the 16-bit addressing or uses less than the 16-bit addressing, (1) reading a switch position of a switch on the memory card; (2) determining an address offset for the address space based on upon the switch position; (3) communicating to the host device via the host controller to use the memory card as one of a plurality of volumes and the address offset.

With respect to the limitation of determining, based on the volume information, whether the initial volume uses a 16- bit addressing or uses less than the 16-bit addressing, accessing the memory card as a single volume when using 32 bit addressing, Colligan discloses **["in step 62, an inquiry is made as to what is the file system type... FAT 32… FAT 16" (col. 4, lines 24-31; fig. 4 and related text) wherein "For example, a 4.3 Gbyte hard disk drive 40 can include a single partition using the FAT 32 file type… For the FAT 32 file type, 4.2 Bbytes can be accessed per partition" (col. 8, lines 4-6; Fig. 2 and related text)]**; where Colligan further teaches partitioning memory into plural volumes when using 16-bit addressing as **["For a similar 4.3 Gbyte hard disk drive 44 of FIG. 3 using a FAT 16 file type, however, the hard disk drive will contain multiple partitions (e.g. C: drive, D: drive and E: drive)" (See fig. 3**

and related text; col. 8, lines 12-19)], and using an offset to access the plural volumes as **[Figure 3 depicts the hard disk utilizing multiple partitions wherein the address range begins at "ADDR. 0" and ends at "ADDR. Max" wherein volumes 34 and 36 are shown, each beginning at an intermediate address within the address space, thus an offset must used from "ADDR. 0" in order to address and access volumes other than the first of the plurality of volumes (See fig. 3 and related text)]**.

With respect to the limitation, (d) when said determining (b) determines that the initial volume uses the 16-bit addressing or uses less than the 16-bit addressing, (1) reading a switch position of a switch on the memory card; (2) determining an address offset for the address space based on upon the switch position; (3) communicating to the host device via the host controller to use the memory card as one of a plurality of volumes and the address offset, Suda discloses **[a memory card comprising plural storage areas (Fig. 1 and related text) wherein "when a FAT 16 is used as the file system, the marginal capacity is equal to 2 gigabytes… the marginal capacity of the entire memory card is equivalent to 8 gigabytes when the memory card includes four storage areas" (par. 0028);** ***thus disclosing a memory card comprising plural storage areas which utilize a FAT 16 file system.*** **Suda further teaches "mechanical switches 16a and 16b for selecting one of the plural storage areas… It is possible to select any one of the storage areas… of the memory card… by use of mechanical switches… For example, when the mechanical switches… are set to positions marked as "1," the controller 10 reflects the state of the switches to the internal register 12a, thereby allowing a memory card host device to handle the first storage area… when… set to position marked as "2", the controller 10 reflects the state of the switches to the internal register 12a, thereby**

allowing the memory card host device to handle the second storage area" (par. 0069; fig. 7 and related text), and explains "the memory card host judges whether or not the memory card has plural storage areas... by a flag in a conventional reserved area of an internal register... the memory card host device switches the storage area so as to refer to a desired storage area. The switching method include... switching by address" (pars. 0033-0034), wherein in figure 5, the address space of memory card beginning at address "00000" wherein a first storage area begins at address "00000," a second storage area begins at address "0FFFF" and a third storage area begins at address "1FFFF" and wherein the address space of the memory card ends at address "xFFFF;" ***therefore in order to address the second storage area and the third storage area, an offset from address "00000" is inherently used*** **(fig. 5 and related text)]**.

Shinomura, Colligan and Suda are analogous art because they are from the same field of endeavor of memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system/method wherein it is determined whether a memory card utilizes a first file system/16-bit file system or a second file system/32-bit file system, formatting and operating the memory card according to the 16-bit file system when it is determined that the memory card utilized the 16-bit file system, and operating the card according to the 32-bit file system when it is determined that the memory card utilizes the 32-bit file system as taught by Shinomura, to divide the address space into multiple volumes when operating the memory card under the 16-bit file system, and to operate the memory card as a single volume when the memory card utilized the 32-bit file system in the manner that Colligan teaches a memory device

is operated as multiple partitions when utilizing a FAT-16 file system, or as a single partition when utilizing a FAT-32 file system since Colligan suggests this would **[enable efficient partitioning of the system into different areas according to the file system used (col. 8, lines 11-14)]**; and to further modify the combination of Shinomura and Colligan to access each of the plurality of volumes based on the position of a switch, wherein an offset is used to access each of the plurality of volumes other than then first volume as taught by Suda, since Suda discloses this would provide benefits as **["it is possible to switch storage areas without adding a new function to the memory card host device if a user designates the storage area by use of mechanical switches. Therefore, it is possible to use all the storage capacity included in the memory card." (par. 0070)]**.

Therefore, it would have been obvious to combine Shinomura with Colligan and Suda for the benefit of creating a method for reading data from a memory card to obtain the invention as specified in claim 72.

7. As per claim 73. (New) A method as recited in claim 72, wherein the switch has at least a first position and a second position, wherein, when the switch position is in the first position and the memory card is operated by dividing the address space of the non-volatile data storage into the plurality of volumes, the first volume of the non-volatile data storage is accessed, and w,herein, when the switch position is in the second position and the memory card is operated by dividing the address space of the non-volatile data storage into the plurality of volumes, a second volume of the non-volatile data storage is accessed **[Suda discloses "mechanical switches 16a and 16b for selecting one of the plural storage areas… It is possible to select any one of the storage areas… of the memory card… by use of mechanical switches… For example, when**

the mechanical switches… are set to positions marked as "1," the controller 10 reflects the state of the switches to the internal register 12a, thereby allowing a memory card host device to handle the first storage area… when… set to position marked as "2", the controller 10 reflects the state of the switches to the internal register 12a, thereby allowing the memory card host device to handle the second storage area" (par. 0069; fig. 7 and related text)].

8. As per claim 74. (New) A method as recited in claim 73, wherein the memory card is formatted into either one of a single volume or a pair of volumes, the pair of volumes being the first volume and the second volume **[Suda teaches memory card may be formatted as having a single storage area or plural storage areas comprising a first and a second area (par. 0033, figs. 6-7 and related text depicting a first and second storage areas). Colligan teaches "in step 62, an inquiry is made as to what is the file system type... FAT 32… FAT 16" (col. 4, lines 24-31; fig. 4 and related text) wherein "For example, a 4.3 Gbyte hard disk drive 40 can include a single partition using the FAT 32 file type… For the FAT 32 file type, 4.2 Bbytes can be accessed per partition" (col. 8, lines 4-6; Fig. 2 and related text)]**.

9. As per claim 75. (New) A method as recited in claim 74, wherein the total non-volatile data storage for the memory card is formatted into the first volume of X gigabytes as the single volume, or formatted into the first and second volumes of X/2 gigabytes each as the pair of volumes **[Colligan discloses "For the FAT32 file type, 4.2 GBytes can be accessed per partition. For the FAT 16 file type, only 2.1 GBytes per partition are allowed" (col. 8, lines 11-13) "For a similar 4.3 Gbyte had disk drive of FIG. 3 using a FAT 16 file type, however, the hard disk drive will contain multiple partitions" (col. 8, lines 14-20, 26-28)]**.

10. As per claim 76. (New) A method as recited in claim 72, wherein said method further comprises: detecting activation of the memory card, and wherein said retrieving (a) and said determining (b) are performed after said detecting detects the activation of the memory card **["Shinomura discloses "When the system is activated, the Socket Service 51 generally establishes a programming interface with both Card Cervices 52 and 61. The presence of the 16-bit Card Service 61 can be detected" (col. 15, lines 3-6). Suda discloses "The memory card is in a state where the power supply is turned on… it is possible to handle the first storage area…. When plural storage areas exist, the area switching module... issues the command to switch storage areas" (par. 0049)]**.

11. As per claim 77. (New) A method as recited in claim 76, wherein the activation of the memory card occurs upon power-on of the memory card or upon insertion of the memory card into a host device **[Shinomura discloses "the client device driver then requests the PC card controller to power the slot. As a result, the PC card is activated as part of the system" (col. 3, lines 59-61). Suda teaches power supply turned on to activate memory card (par. 0049)]**.

12. As per claim 78. (New) A method as recited in claim 72, wherein the memory card is formatted into a single volume or a plurality of volumes, and wherein the total non-volatile data storage for the memory card is formatted into the first volume of X gigabytes as the single volume, or formatted into the N volumes of X/N gigabytes each as the plurality of volumes **[Colligan discloses "For the FAT32 file type, 4.2 Gbytes can be accessed per partition. For the FAT 16 file type, only 2.1 Gbytes per partition are allowed" (col. 8, lines 11-13) "For a similar 4.3 Gbyte had disk drive of FIG. 3 using a FAT 16 file type, however, the hard disk drive will contain multiple partitions… the C:drive partition may include a 2.1 Gbyte**

partition, the D:drive partition a 16Bbyte partition, and the E:drive partition a 500 MByte partition… Other partitioning… is possible" (col. 8, lines 14-20, 26-28)].

13. As per claim 79. (New) A method as recited in claim 72, wherein when said determining (b) determines the initial volume uses greater than the 16-bit addressing, the initial volume has a FAT-32 file format **[Shinomura discloses 16-bit addressing mode and 32-bit addressing mode (col. 7, lines 24-65). Colligan discloses "in step 62, an inquiry is made as to what is the file system type... FAT 32… FAT 16" (col. 4, lines 24-31; fig. 4 and related text)]**.

14. As per claim 80. (New) A method as recited in claim 72, when said determining (b) determines that the initial volume uses the 16-bit addressing or uses less than the 16-bit addressing, each of the multiple volumes has a FAT-16 file format **[Shinomura discloses 16-bit addressing mode and 32-bit addressing mode (col. 7, lines 24-65). Colligan discloses "in step 62, an inquiry is made as to what is the file system type... FAT 32… FAT 16" (col. 4, lines 24-31; fig. 4 and related text)]**.

ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Response to Amendment

15. Applicant's arguments filed on 6/28/2010 with respect to claims have been fully considered but are moot in view of the new ground(s) of rejection.

CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

16. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

17. Per the instant office action, claims 72-80 have received an action on the merits and are subject to a non-final rejection.

a(2) CLAIMS REJECTED IN THE APPLICATION

18. Claims 1-71 have been canceled.

b. DIRECTION OF FUTURE CORRESPONDENCES

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

20. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions

on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

November 1, 2010

/Yaima Campos/
Examiner, Art Unit 2185